



## STB75NH02L

N-Channel 24V - 0.0062Ω - 60A - D<sup>2</sup>PAK  
STripFET™ III Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB75NH02L	24V	<0.008Ω	60A <sup>(1)</sup>

1. Limited by package

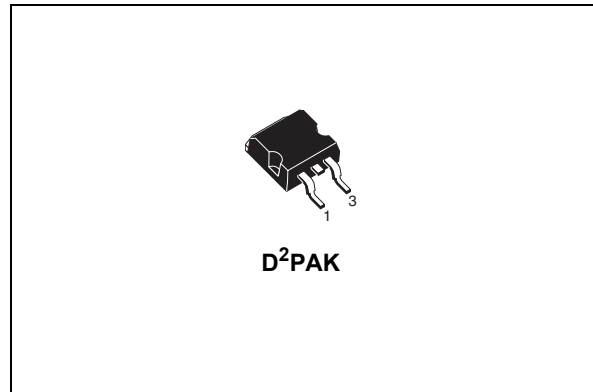
- R<sub>DS(ON)</sub> \* Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

### Description

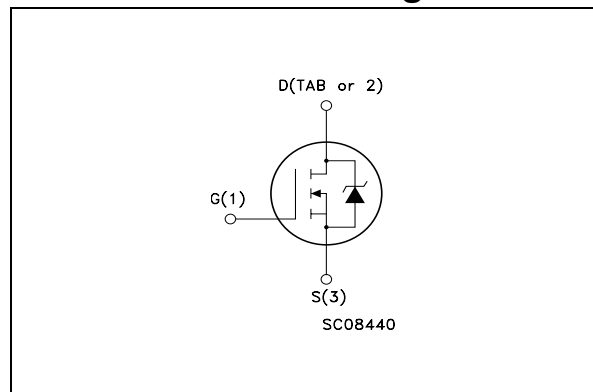
The device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STB75NH02LT4	B75NH02L	D <sup>2</sup> PAK	Tape & Reel

## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
$V_{\text{DS}}$	Drain-source voltage ( $V_{\text{GS}} = 0$ )	24	V
$V_{\text{GS}}$	Gate-source voltage	$\pm 20$	V
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	60	A
$I_{\text{D}}$	Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$	53	A
$I_{\text{DM}}^{(3)}$	Drain current (pulsed)	240	A
$P_{\text{TOT}}^{(4)}$	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	80	W
	Derating factor	0.53	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(5)}$	Single pulse avalanche energy	360	mJ
$T_{\text{J}}$ $T_{\text{stg}}$	Operating junction temperature storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Guaranteed when external  $R_{\text{g}} = 4.7\Omega$  and  $t_{\text{f}} < t_{\text{fmax}}$
2. Value limited by wire bonding
3. Pulse width limited by safe operating area
4. This value is rated according to  $R_{\text{thJC}}$
5. Starting  $T_{\text{J}} = 25^{\circ}\text{C}$ ,  $I_{\text{d}} = 30\text{A}$ ,  $V_{\text{dd}} = 15\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{\text{thJC}}$	Thermal resistance junction-case max	1.88	$^{\circ}\text{C}/\text{W}$
$R_{\text{thJA}}$	Thermal resistance junction-amb max	62.5	$^{\circ}\text{C}/\text{W}$
$T_{\text{I}}$	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25\text{ mA}$ , $V_{GS} = 0$	24			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 20\text{ V}$ , $V_{DS} = 20\text{ V}$ , $T_c = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1	1.8		V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 30\text{ A}$ $V_{GS} = 5\text{ V}$ , $I_D = 30\text{ A}$		0.0062 0.008	0.008 0.014	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 18\text{ A}$		27		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 15\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		2050 545 70		pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 10\text{ V}$ , $I_D = 60\text{ A}$ $V_{GS} = 5\text{ V}$ <i>Figure 14</i>		17 7.7 3.5	22	nC nC nC
$R_G$	Gate Input Resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.1		$\Omega$

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time rise time	$V_{DD} = 10\text{ V}$ , $I_D = 30\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ <i>Figure 15</i>		12 200		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time fall time	$V_{DD} = 10\text{ V}$ , $I_D = 30\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ <i>Figure 15</i>		18 25		ns ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				60	A
$I_{SDM}$	Source-drain current (pulsed)				240	A
$V_{SD}^{(1)}$	Forward on Voltage	$I_{SD} = 30 \text{ A}, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=60 \text{ A}, di/dt = 100\text{A}/\mu\text{s},$ $V_{DD}=15 \text{ V}, T_J=150^\circ\text{C}$		36		ns
$Q_{rr}$	Reverse recovery charge			35		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			3.6		A

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

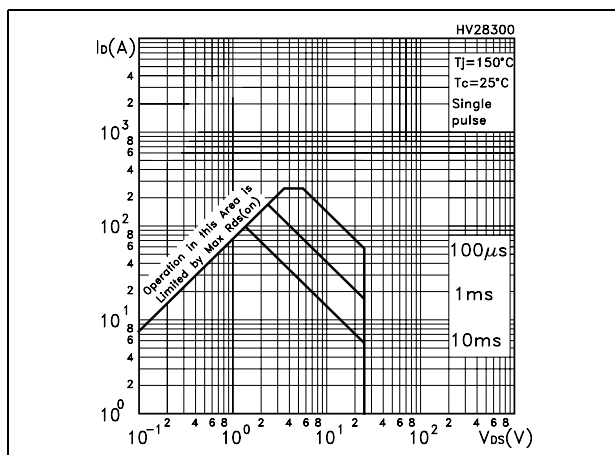


Figure 2. Thermal impedance

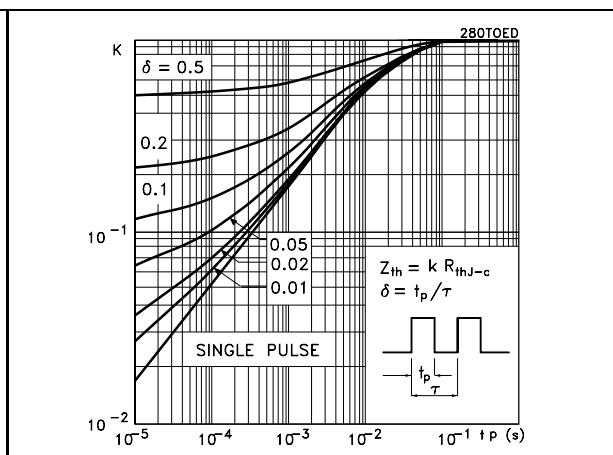


Figure 3. Output characteristics

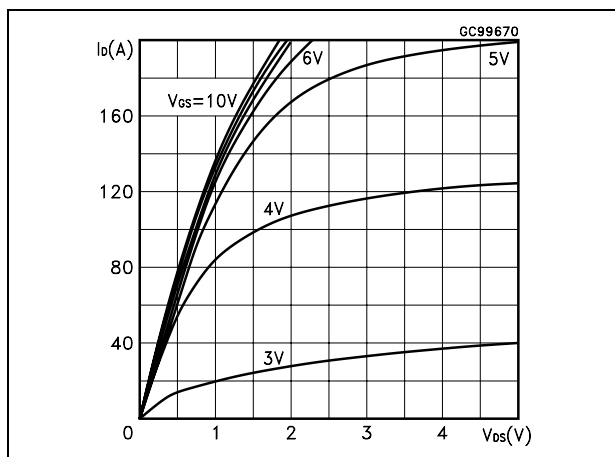


Figure 5. Transfer characteristics

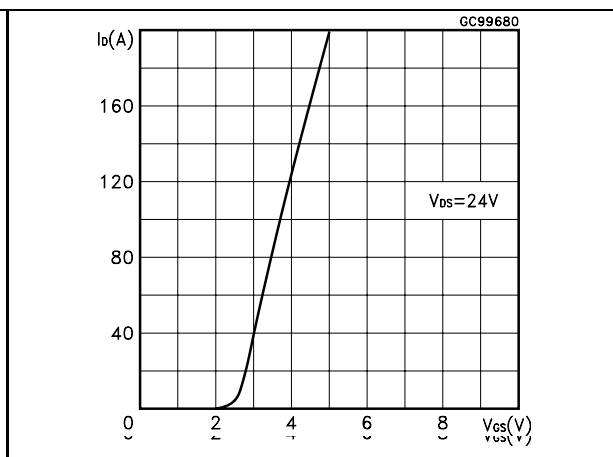


Figure 4. Transconductance

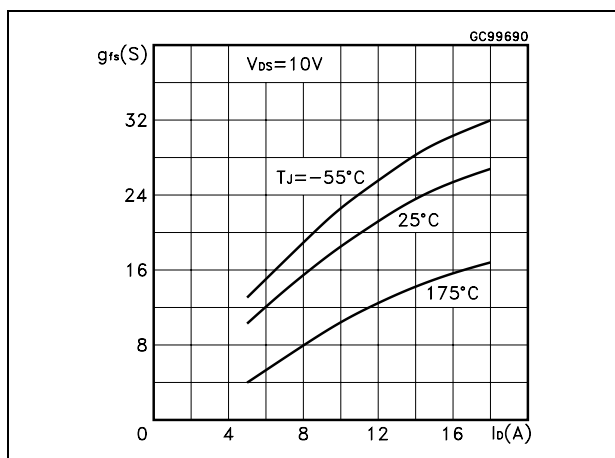


Figure 6. Static drain-source on resistance

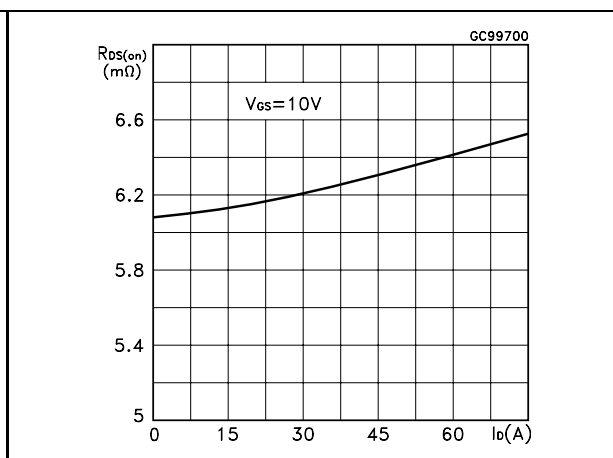


Figure 7. Gate charge vs gate -source voltage Figure 10. Capacitance variations

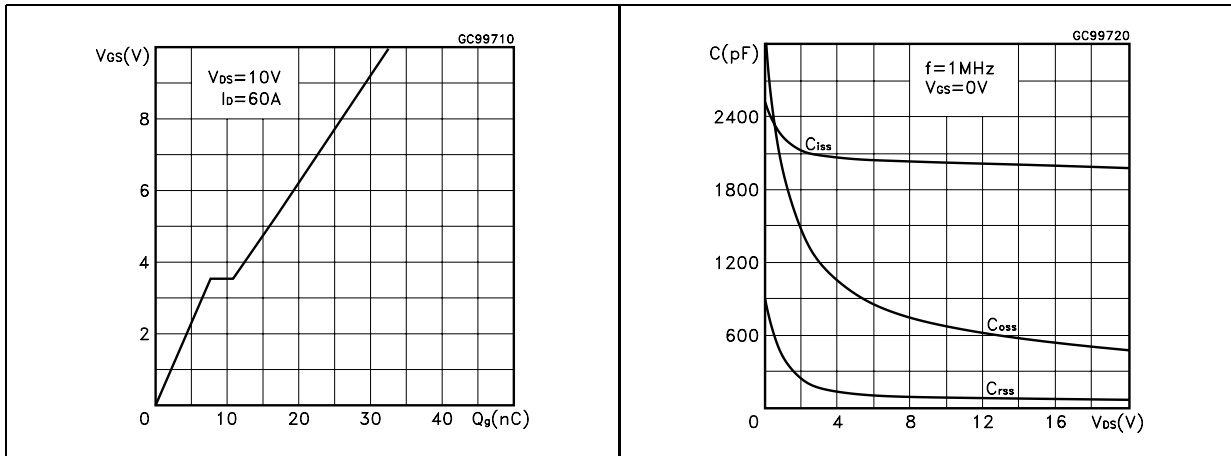


Figure 8. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs Temperature

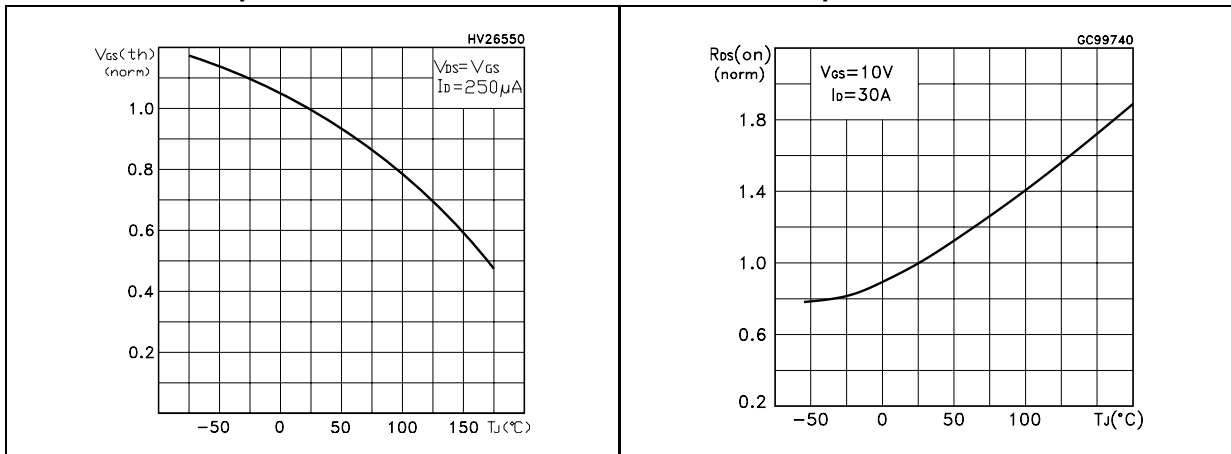
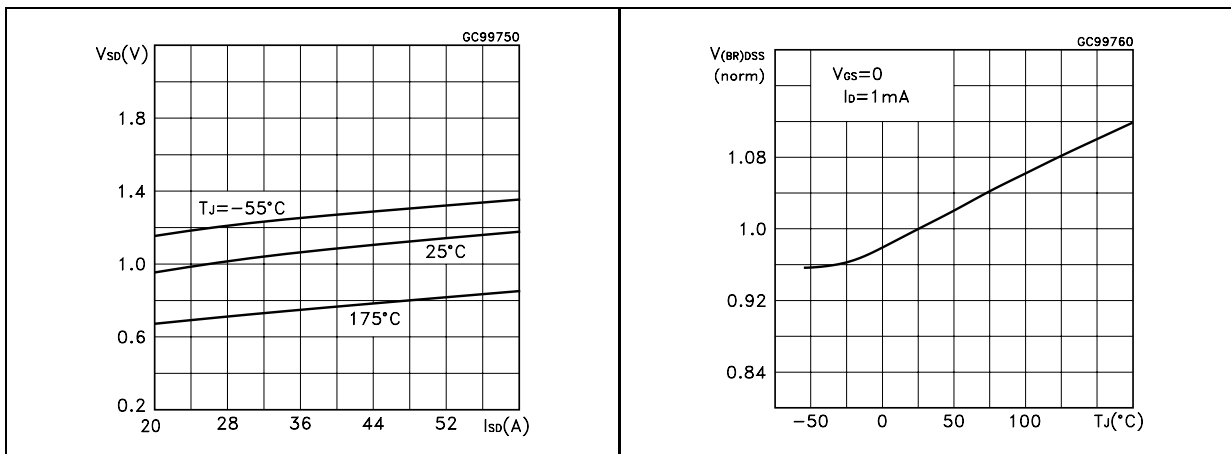
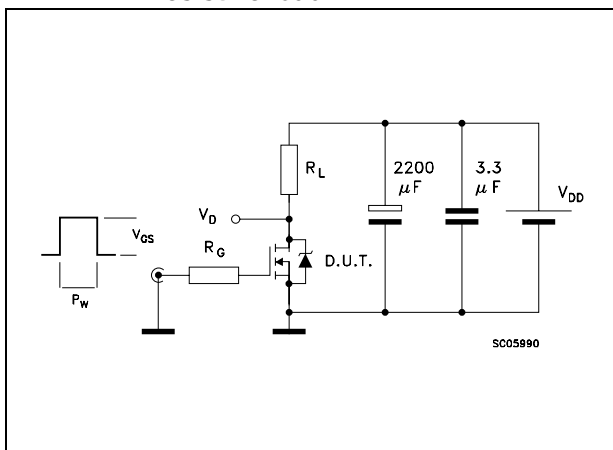


Figure 9. Source-drain diode forward characteristics Figure 12. Normalized BVDSS vs temperature

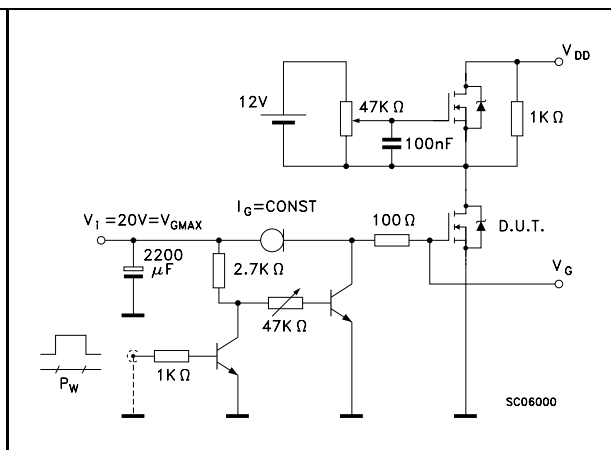


### 3 Test circuits

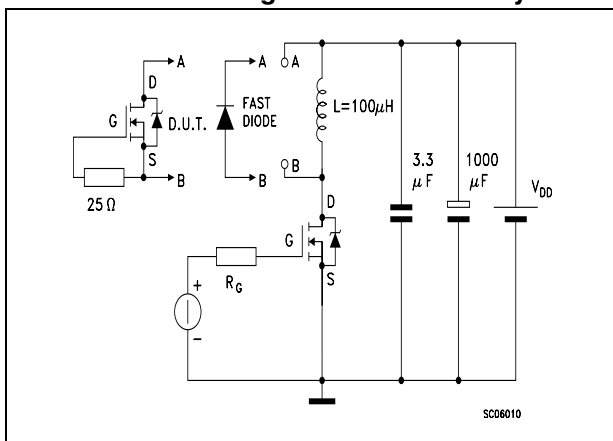
**Figure 13. Switching times test circuit for resistive load**



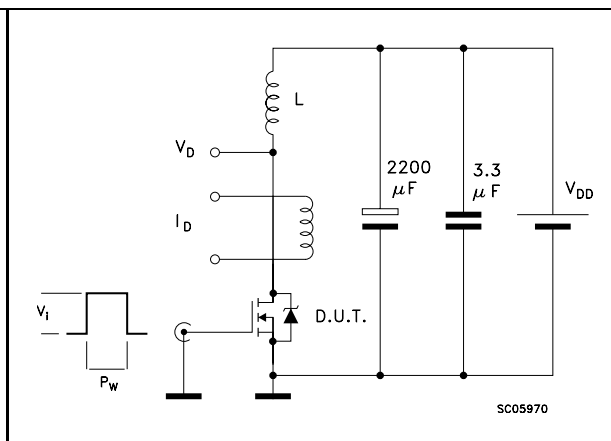
**Figure 14. Gate charge test circuit**



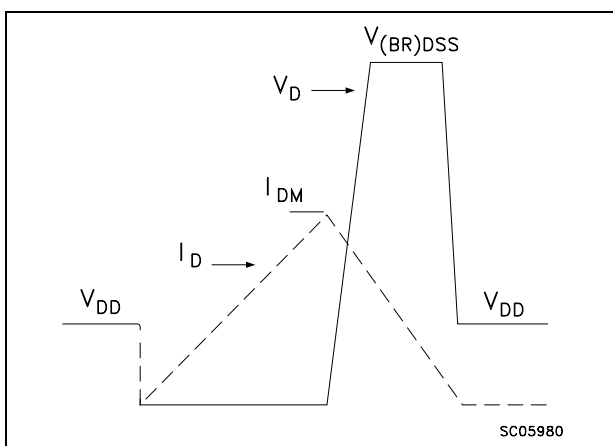
**Figure 15. Test circuit for inductive load switching and diode recovery times**



**Figure 17. Unclamped inductive load test circuit**



**Figure 16. Unclamped inductive waveform**



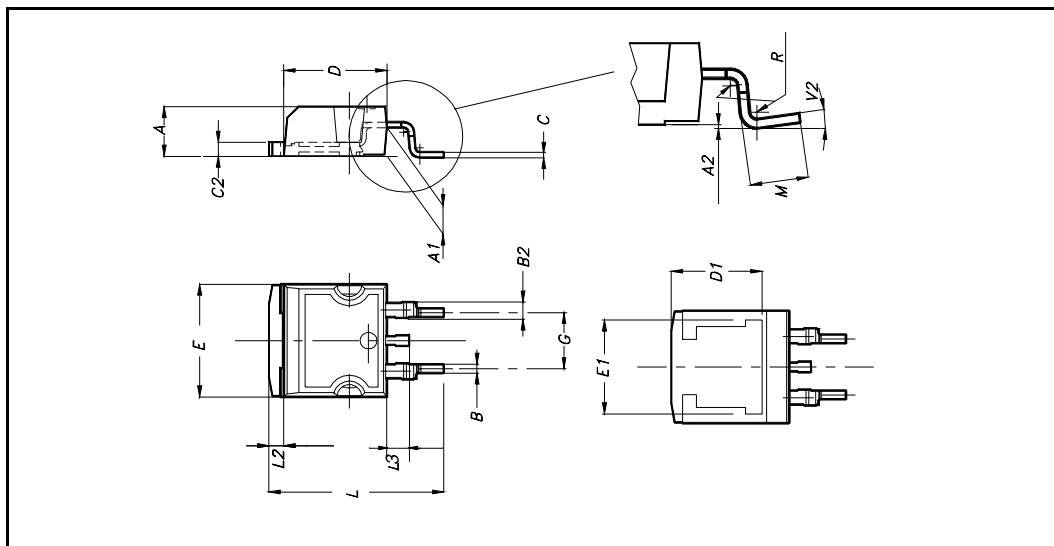


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

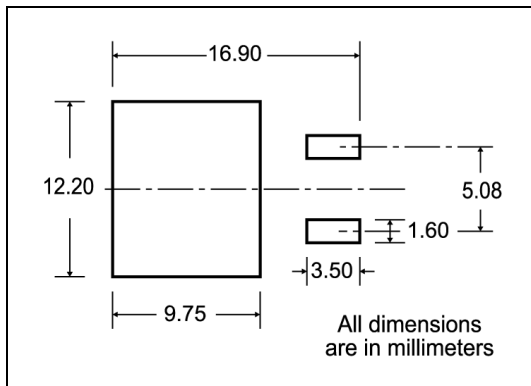
**D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



# 5 Packing mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

\* on sales type

## 6 Revision history

**Table 7. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
24-Oct-2005	1	Preliminary version
15-Mar-2006	2	Complete version
22-Jul-2006	3	New template, no content change

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